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L4	6404	(wire or cable) near rout$3	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/09/18 16:31
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L6	104	L5 and Cad	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/09/18 16:42
L7	317	((wir$3 or cabl$3) near route) and (cad or cae or (computer adj aided))	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/09/18 16:54
L8	31	((wir$3 or cabl$3) near (clamp or fastener)) and (cad or cae or (computer adj aided))	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/09/18 17:25
L9	2	"5021968".pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/09/18 17:23
L10	15	("5021968").URPN.	USPAT	OR	OFF	2005/09/18 17:23
L11	12	((wir$3 or cabl$3) near (hanger$1)) and (cad or cae or (computer adj aided))	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/09/18 17:26

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Brady, H.N.; Blanks, J.;
Proceedings of the IEEE
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Grinberg, J.; Hart, J.; Horel, T.; Wen-Jay Hsu; Kaku, J.; Chin Kim; Song Kim; K
H.; Lauterbach, G.; Lo, R.; McIntyre, H.; Mehta, A.; Murata, D.; Nguyen, S.; Ye
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IEEE Std 1481-1999
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for random sampling **and** oblivious packet **routing**. 1 Introduction The most fundamental tools used the tail probabilities of the sums of bounded **and** independent random variables. We present a simple
cs.nyu.edu/cs/faculty/siegel/Limited.ps

The Post Office Experience: Designing a Large Asynchronous.. - Davis, Stevens, Coates (1993) (Correct) (43 citations)
circuitry takes up 45%pads cover 11%**wire routing** requires 19%and the other 6% is unused space and complex device would be well supported by our **CAD** capability. What follows is a brief description of synthesize the AFSMs. Since we were not experienced **CAD** people, we grossly underestimated the need to pay
www.cs.utah.edu/~ald/hicss.ps

Rectilinear Paths among Rectilinear Obstacles - Lee, Yang, Wong (1996) (Correct) (12 citations)
fields, such as motion planning in robotics, **wire routing** in VLSI and logistics in operations research. Computed-Aided Design for PCB or VLSI circuit **routing, wires** and modules are usually restricted to lie on Antognetti, A tile-expansion router,IEEE Trans. **CAD**, Vol.**CAD**-6, no.4, 1987, 507-517. 45] K. M.
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FPGA Routing Architecture: Segmentation and Buffering to.. - Betz, Rose (1999) (Correct) (8 citations)
routing architecture. Pass transistor Routing **wire routing** switch Tri-state buffer routing switch Logic defines such features as: 1. The length of each **routing wire** segment (how many logic blocks a **routing wire** less accurate, delay and area metrics. Third, the **CAD** flow we use to evaluate architectures employs a
www.eecg.toronto.edu/~jayar/pubs/betz/fpga99betz.ps.gz

Physical Hierarchy Generation with Routing Congestion Control - Chang, Cong, Pan, Yuan (2002) (Correct) (5 citations)
bounding box wire length but 3 6% shorter **routing wire** length measured by graph based A-tree. Handling High Complexity Designs In The Vlsi **Cad** Area [16, 17, 18]The Backbone Of Our System Is A
ballade.cs.ucla.edu/~cong/papers/p64-chang.pdf

Logic Synthesis for Cellular Architecture FPGA using BDD - Lee (1997) (Correct) (4 citations)
d) is not a Maitra term and it needs another **routing wire** to be realized in the cellular
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A Negative Reinforcement Method for PGA Routing - Lewis, Wang (1993) (Correct) (3 citations)
as well as leading to shorter overall **routing wire** length. This paper is organized as follows. Lewis and Wang 2 After the specification stage, the **CAD** process for FPGA's proceeds through logic Technique for Global Wiring.IEEE Trans. on **CAD**, vol. **CAD**-6, no. 2, March 1987, 165-172. NRT86
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Parallel Algorithms for VLSI Circuit Extraction - Belkhale, Banerjee (1991) (Correct) (3 citations)
circuit extraction, cell placement and **wire routing** will increase tremendously. There will be an Orders Of Magnitude Performance Improvements In Vlsi **Cad** Applications. In This Paper, We Propose Parallel the computational requirements of performing various **CAD** tasks such as simulation, design-rule checking,
www.ece.nwu.edu/cpdc/ProperCAD/tcad91.bb.ps.Z

Mixing Buffers and Pass Transistors in FPGA Routing Architectures - Sheng, Rose (2001) (Correct) (2 citations)
of an FPGA consists of: 1. The length of each **routing wire** in the FPGA measured in terms of number of as follows: Section 2 outlines the experimental **CAD** flow which is used to profile the previous Figure 2 illustrates the empirical methodology and **CAD** flow used to evaluate routing architectures. It is
www.eecg.toronto.edu/~jayar/pubs/sheng/shengfpga01.ps

Automated Detection of Pulmonary Nodules in Helical.. - Lee, Hara, Fujita.. (2001) (Correct) (2 citations)
applied to such optimization problems as **wire routing**, scheduling, adaptive control, game playing, to develop a technique for computer-aided diagnosis (**CAD**) systems to detect lung nodules in helical X-ray

that our scheme can be regarded as a technique for **CAD** systems to detect nodules in helical CT pulmonary
www.isi.uu.nl/Meetings/../TGV/Lee01a.pdf

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Parallel Algorithms For **Cad** With Applications To Circuit Extraction By Krishna
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www.ece.nwu.edu/cpdc/ProperCAD/phd90.b.ps.Z

Circuit Design of Routing Switches - Guy Lemieux University (2002) (Correct) (1 citation)
each transistor in the cluster, including the **routing. Wire** RC values are determined from the tile size
used for the HSPICE simulations in Section 3 and the **CAD** flow in the later sections. 2.1 HSPICE Circuit
V. Betz, J. Rose, and A. Marquardt, Architecture and **CAD** for Deep-Submicron FPGAs. Boston: Kluwer
Academic
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Wire Routing and Satisfiability Planning - Erdem, Lifschitz, Wong (2000) (Correct) (1 citation)
Wire Routing and Satis ability Planning Esra Erdem,
research and development in computer-aided design (**CAD**) software is very active in both industry and
and academia. Routing is an important step in **CAD** for VLSI circuits [7]It is the problem of
www.cs.utexas.edu/users/esra/papers/cl00.ps

More on Wire Routing with ASP - East, Truszczynski (2001) (Correct) (1 citation)
More on **Wire Routing** with ASP Deborah East and Mirosl/aw Truszczy
size of circuits, research in computer aided design (**CAD**) for VLSI is an active area of research. In a
www.cs.nmsu.edu/~tson/ASP2001/16.ps

ETDD-based Synthesis of Term-Based FPGAs for Incompletely.. - Lee, Drechsler (1998) (Correct) (1 citation)
be implemented in a cell array without extra **routing wire**. Example 1 1. A logic expression (ab)cd can
www.informatik.uni-freiburg.de/~drechsle/ps_test/ETDDSYNTH.ps

Succinct Representation of Graphs - Project Report For (Correct)
analysis)minimum spanning forest (used in **wire routing** and layout) are of interest. 3.1 Small
The Primary Target For These Models Were Vlsi **Cad** Applications. In This Project We Show That One Of
To Reduce The Space And Time Complexity Of Vlsi **Cad** Applications. Although Bdds Have Several Desirable
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Optimized Pin Assignment for Lower Routing Congestion - After Floorplanning Phase (Correct)
optimization goal is generally to reduce the **routing wire** length and/or the circuit area. Permission to
www.cs.ucla.edu/~mrivero/PAPER/p17-zhang.pdf

Concurrent Product Design: A Case Study On The Pico Radio Test.. - Odell, Wright (2002) (Correct)
gap around the PCB stack to allow for **wire routing** and antenna placement. Four long screw bosses
access to the board stack components. **Wire Routing Wire routing** is often an overlooked aspect in
o Tes Bed Cas ing Cover Serial Port Window Figure 2: **CAD** model of PRTB version 1 assembly 3 Copyright
everandever.com/dan/publications/DETC2002_DFM-34154.pdf

Unknown - (Correct)
wiring rule checking, component placement and **wire routing**. Computers have been used to a lesser extent
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